UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

23373 7590 08/21/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

MAIL DATE	DELIVERY MODE
08/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008 and 19 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,16 and 29-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14, 16 and 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/18/08 has been entered.

Response to Amendment

2. Amendment filed 6/19/08 under 37 C.F.R. 1.116 has been entered following the filing of aforementioned Request for Continued Examination. Said Amendment forms the basis for this Office Action. In said Amendment Applicant substantially amended claims 14, 16 and 29-35 through substantial amendment of claim 19. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 29, 16 and 34-35*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Osamu Nakamura (JP

2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited), Adler et al (5,757,050) (previously cited) and Smith (6,255,180 B1).

On claim 29: Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304 *capable* of being driven by low voltage) formed above said insulating substrate (cf. Figure 1), comprising a first active layer 302 (island-like portion to the left in Figure 1 comprising 305a; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307 *capable* of being driven by high voltage) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1 comprising 305b; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) and capable of being driven at high voltage being formed on said second gate insulating film,

wherein said second gate insulating film 303/306 comprises said first gate insulating film 303 (Figure 1) and a gate cover 306 (Figure 1 and [0005]) formed above said first gate insulating film (loc.cit and Figure 1),

wherein said second active layer has at least two impurity doping regions 305b on both sides of the channel ([0005]).

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) said "at least two impurity doping regions" are "formed in a self-aligning manner with respect to said first gate electrode" and "so as to overlap said first gate electrode by 0.1 μm or less";

(b) "wherein said second thin film transistor further comprises a third gate electrode driven at low voltage and formed between said second active layer and said second gate electrode with gate length shorter than that of the second gate electrode"; nor

(c) "wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode".

With regard to limitation (a), *the limitation "formed in a self-aligning manner with respect to said gate electrode"* only has patentable weight in the result for the final structure and constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See MPEP 2113, from which it is clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process.

Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions.

In addition, it would have been obvious to include the limitation "*so as to overlap said first gate electrode by 0.1 μm or less"* in view of Adler et al, who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 μm or less (col. 8, l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode (13 or 23) between an active layer and a gate electrode (17 or 27) with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Furthermore, gate electrode 17 or 27 by Nakamura et al has a length that exceeds the length of gate electrode 13 (see front Drawing, upper portion, and see Drawing 2, upper portion) and hence the range limitation on gate lengths is met in the

Prior Art as cited. A *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties.

Finally, it would have been obvious to include limitation (c) as defined above, in view of Nakamura and Smith:

Nakamura teaches through Drawing 2 and discussion (see computerized translation made of record by examiner, especially paragraphs [0049]-[0051]), showing impurity LDD doping region 21k existing between the second gate electrode and the third electrode in as far as its coordinate parallel to the upper main surface is concerned. As is clear from Nakamura's discussion, the relative horizontal extent of said LDD doping region is a matter of design, whereby in the case of Drawing 2 the electric field in said LDD region is weakened relative to the field caused by the third gate electrode in the active layer (loc.cit.), thus reducing the hot electron effect further, which provides motivation towards adopting the teaching by Nakamura through the embodiment of Drawing 2 in this regard. Although Nakamura does not necessarily teach said impurity doping region to be disposed NOT directly below either said second gate electrode or said third gate electrode, it would have been obvious to avoid positioning impurity doping region 21k in Nakamura directly below either of said second and third gates so as to further mitigate the short-channel effect, as witnessed for instance by Smith, who, in a patent on MOS transistors with LDD regions (see title, abstract, "Field of the Invention", and "Description of the Related Art"), hence analogous art, teaches

not to position the LDD regions 20 below, and directly adjacent to, gate conductors (see col. 2, l. 11-40, and Figure 1: especially col. 2, l. 28-40), which consideration evidently prompt his own design of graded junctions 62 positioned not directly below gate electrodes (see Figure 2). Because the second gate electrode in the AAPA and in Nakamura is a high-voltage gate electrode "below" and "directly adjacent" applies to both the second and third gate electrode in the spirit of the teaching by Smith, because what is important is the field effect. Motivation to further includes the teaching by Smith in the teachings by Nakamura and thereby in those of the AAPA derives immediately from the well-known adverse consequences of short-channel effects on achievable currents: see in this regard Smith, col. 2, l. 38-40).

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by Applicant because LDD regions counteract hot electron effects. *Motivation* to include the teaching on LDD structure by *Nakamura* is the avoidance of hot electron effects in the high-voltage transistor.

On claim 34: said first gate electrode 304, said second gate electrode 307 in the prior art as admitted by applicant are formed under wires which connect to said impurity doping regions 305a and 305b, respectively. Inclusion of the third gate electrode (as shown would have been obvious over Nakamura) necessarily places said gate electrode between the active layer and the second gate electrode according to claim 29

and hence places said third gate electrode also under said wires that connect to said impurity doping regions.

On claim 35: in the combined invention, said impurity doping region 21k between the second gate electrode and the third gate electrode is an LDD region (see Nakamura et al. [0049]-[0051]) (see also rejection of claim 29, in which this is also pointed out).

2. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura, Adler et al and Smith as applied to claim 29 above, and further in view of Zhang et al (6,507,069 B1) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant in view of Nakamura, Adler et al and Smith, none of the above references, however, necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current (col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

3. ***Claim 30*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura, Adler et al and Smith as applied to claim 29, and further in view of Izawa et al (5,053,849) (previously cited).

As detailed above, claim 29 is unpatentable in view of Prior Art as Admitted by Applicant, in view of Nakamura, Smith and Adler et al. None of these references necessarily teach the further limitation defined by claim 30. *However, it would have*

been obvious to include the further limitation in view of Izawa et al, who, in a patent on overlapping gate/drain gate structures (see title), hence analogous art, teach the overlap to be about 0.2 μm (col. 13, l. 53-66), which overlaps the range as claimed. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

4. ***Claims 31-32*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura, Smith and Adler et al as applied to claim 29, in further view of Numasawa et al (6,048,795) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant, in view of Nakamura, Adler et al and Smith. None of these reference necessarily teach the further limitation defined by claim 31. *However, it would have been obvious to include the further limitation ad (c) in view of Numasawa et al*, who, in a patent on gate electrodes formed in a self-alignment process step with source and drain regions (see Figure 2E and col. 1, l. 17-52), hence analogous art, teach the gate electrode to comprise a two –layer structure including a semiconductor layer 13 (hence claim 32 is also met) and a metal layer 14 (col. 3, l. 25 – col. 4, l. 58). *Motivation* to include the teaching by Numasawa et al in the invention of the Prior Art derives from the advantage of increased electric conductivity of the gate electrode without having to give up the convenience of the self-

alignment process step in creating source and drain regions with the gate as mask (col. 1, l. 16-30).

5. ***Claim 33*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura, Adler et al and Smith as applied to claim 29 above, and further in view of Suzawa et al (5,914,498) (previously cited).

As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant, in view of Nakamura and Adler et al. None of these references necessarily teach:

(A) the further limitation that said third gate electrode is formed of the same material as said first gate electrode; nor the further limitation;

(B) that said third gate electrode has the same thickness as said first gate electrode. *However, it would have been obvious to include the limitations (A) and (B) in view of Suzawa et al*, who teach gate electrodes displaced substantially laterally from each other to be made of the same material (aluminum 105/106: Figure 1A and col. 5, l. 20-27) and to have the same thickness (as witnessed by the reference to the thickness of the gate electrodes: see col. 14, l. 68 and col. 15, l. 1). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416; and, furthermore, that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such

that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05[R-5].

Response to Arguments

6. Applicant's arguments filed 6/19/08 in Remarks have been fully considered but they are not persuasive. Although the rejections under 35 USC 112, first and second paragraph, have been overcome by amendment, the substantial amendment to the claims fails to place the application in condition for allowance: counter to applicant's argument that it would not have been obvious to so position the impurity doping region and gate electrodes, the newly added limitation on the placement of the impurity doping region NOT directly below either the second or third gate electrode would have been obvious so as to suppress short-channel effects and their resulting deterioration of current performance, as can be witnessed for instance by Smith (US 6,255,180 B1), as explained in detail in the rejections overhead, which are herewith included by reference in their entirety.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663